

### **REMARKS**

Claims 1-16, 37-66, 85-90, and 99-101 are pending, with claims 1-16, 51-66, and 99-101 rejected, and claims 37-50 and 85-90 withdrawn from consideration.

Claims 1-16, 51-66, and 99-101 remain rejected under 35 U.S.C. § 102(e) as being anticipated by Sharrit et al. (U.S. Patent No. 5,999,990; hereinafter “Sharrit”).

Applicant continues to traverse this rejection for the reasons stated in the Amendment filed September 3, 2008. The “Remarks” from this previous Amendment are incorporated herein by reference in their entirety.

In the final Office Action, page 2, “Response to Arguments” section, the Examiner asserts that he disagrees with Applicant’s position that the claims recite that the at least one kernel operates autonomously not only with respect to other kernels but also with respect to all other circuitry. As support for his position, the Examiner asserts the following:

Since the contents, such as “operates autonomously with respect to all other circuitry”, “independently from any circuitry outside of the computing element”, and/or “independently of a system processor” are not included in the claims, even though the limitation “with respect to the other of the plurality of kernels” was removed from the claims, the claimed limitation “the at least one kernel to operate autonomously” still could be interpreted “the at least one kernel to operate autonomously with respect to the other of the plurality of kernels” or “the at least one kernel performs any operation performed independently from the other plurality of kernels not necessarily independently from a system processor” as pointed by the Board.

Applicant respectfully disagrees with the Examiner position. The Board addressed the language “operate autonomously with respect to the other of the plurality of kernels.” Contrary to the Examiner’s suggestion, the Board did not address the current claim language.

Independent claim 1 currently recites the “local controller permitting the at least one kernel to operate autonomously.” Similarly, independent claim 51 currently recites “the local controller architecture ... permitting the at least one kernel architecture to operate autonomously.” The at

least one kernel operating autonomously is absolute, that is, there is no qualifying language. For the Examiner to interpret the claims to recite “the at least one kernel to operate autonomously with respect to the other of the plurality of kernels” or “the at least one kernel performs any operation performed independently from the other plurality of kernels not necessarily independently from a system processor” is to read into the claims limitations that do not exist. This is improper.

Even if the Examiner’s position with respect to independent claims 1 and 51 were proper, the Examiner’s arguments would still not be proper with respect to dependent claims 99-101. Dependent claims 99-101 recite that “the local controller permits the at least one kernel to operate autonomously with respect to the other of the plurality of kernels *and any other circuitry within the [processor (claim 99) / communication device (claim 100) / electronic device (claim 101)].*” Thus the Examiner’s statement above that recitations such as “operates autonomously with respect to all other circuitry,” “independently from any circuitry outside of the computing element”, and/or “independently of a system processor” are not included in the claims, is not correct, as it is explicitly recited in the dependent claims.

During the February 11, 2009 telephone interview, the Examiner asserted that the claimed local controller in the hardware kernel must somehow be under the control of microprocessor 112 and allocator 219, as shown in Figure 2A of the application. The Examiner also referred Applicant to paragraphs [0073] and [0099].

Applicant also disagrees with this position. In the present application the kernels have different modes of operation. In the autonomous mode the kernels are not under the control of microprocessor 112 and allocator 219. A more detailed explanation follows.

Hardware kernels 261a-266a are grouped in a hardware kernel plane 201a. In hardware kernel plane 201a, there is one internal bus 204a coupling all hardware kernels 261a-266a of hardware kernel plane 201a. The internal bus 204a of hardware kernel plane 201a permits communication of status, measurement, and control information among hardware kernels 261a-266a in the same hardware kernel plane 201a. See Figure 2C. A hardware kernel 261a-266a is also

coupled to configuration bus 206a, which is in turn coupled to allocator 219, and ultimately microprocessor 112, of Figure 2A.

During operation, control of a hardware kernel 261a-266a could be provided by (a) an external controller; (b) the hardware kernel itself using local controller 271 in an autonomous mode; or (c) another hardware kernel 261a-266a in the same hardware kernel plane 201a.

When a hardware kernel 261a-266a runs in the autonomous mode, it does not use internal bus 204a of hardware kernel plane 201a to receive control information. However the hardware kernel 261a-266a may use this internal bus 204a to transmit status, measurement, and control information targeted to another hardware kernel 261a-266a or to a controller.

Alternatively, when a hardware kernel 261a-266a is not running in autonomous mode, there are two possible modes. The first mode is when the hardware kernel 261a-266a is under the control of the controller via hardware kernel plane's internal bus 204a and external bus 206a. The second mode is when the hardware kernel 261a-266a is under the control of another hardware kernel in the same hardware kernel plane 201a via the plane's internal bus 204a.

The claims are directed to the autonomous mode in which the kernel 261a-266a operates autonomously using its own local controller 271. As discussed above, during this mode local controller 271 does not receive control information from microprocessor 112 or allocator 219.

Claims 1-16, 51-66, and 99-101 are therefore patentable over Sharrit for at least these reasons. Reconsideration and withdrawal of the prior art rejection is therefore respectfully requested.

In view of the above, Applicant believes the pending application is in condition for allowance.

In the event a fee is required or if any additional fee during the prosecution of this application is not paid, the Patent Office is authorized to charge the underpayment to Deposit Account No. 50-2215.

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Respectfully submitted,

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